74LVC3G14

Triple inverting Schmitt trigger with 5 V tolerant input

Rev. 06 — 7 February 2008 Product data sheet

1. General description

The 74LVC3G14 provides three inverting buffers with Schmitt trigger action.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment. Schmitt trigger action at the inputs makes the circuit tolerant of slower input rise and fall time. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Unlimited rise and fall times
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

3. Applications

- Wave and pulse shaper for highly noisy environment
- Astable multivibrator
- Monostable multivibrator.

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G14DP	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G14DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G14GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC3G14GM	−40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

5. Marking

Table 2. Marking codes

Type number	Marking code
74LVC3G14DP	V14
74LVC3G14DC	V14
74LVC3G14GT	V14
74LVC3G14GM	V14

6. Functional diagram

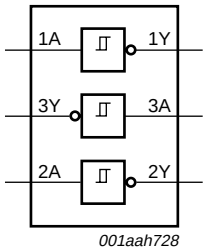


Fig 1. Logic symbol

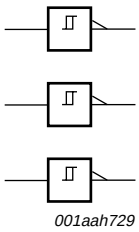


Fig 2. IEC logic symbol

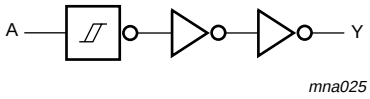


Fig 3. Logic diagram (one Schmitt trigger)

7. Pinning information

7.1 Pinning

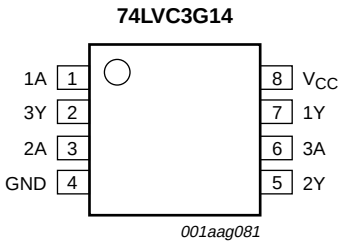
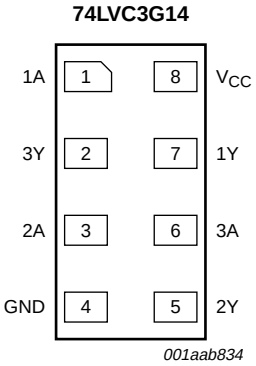
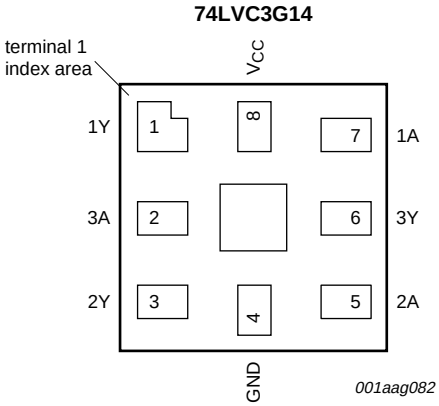


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)



Transparent top view

Fig 5. Pin configuration SOT833-1 (XSON8)



Transparent top view

Fig 6. Pin configuration SOT902-1 (XQFN8U)

7.2 Pin description

Table 3. Pin description

Symbol (n = 1, 2, 3)	Pin		Description
	SOT505-2, SOT765-1 and SOT833-1	SOT902-1	
nA	1, 3, 6	7, 5, 2	data input
nY	7, 5, 2	1, 3, 6	data output
GND	4	4	ground (0 V)
V_{CC}	8	8	supply voltage

8. Functional description

Table 4. Function table [1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1][2]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1][2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	250	mW
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 and VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		–40	+125	°C

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	µA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	0.1	10	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	3.5	-	pF
T_{amb} = −40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.7	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.8	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±20	µA

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±20	µA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	-	40	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	µA

[1] All typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

Table 8. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 8

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Figure 9 and Figure 10						
		V_{CC} = 1.8 V	0.70	1.10	1.50	0.70	1.70	V
		V_{CC} = 2.3 V	1.00	1.40	1.80	1.00	2.00	V
		V_{CC} = 3.0 V	1.30	1.76	2.20	1.30	2.40	V
		V_{CC} = 4.5 V	1.90	2.47	3.10	1.90	3.30	V
		V_{CC} = 5.5 V	2.20	2.91	3.60	2.20	3.80	V
V_{T-}	negative-going threshold voltage	see Figure 9 and Figure 10						
		V_{CC} = 1.8 V	0.25	0.61	0.90	0.25	1.10	V
		V_{CC} = 2.3 V	0.40	0.80	1.15	0.40	1.35	V
		V_{CC} = 3.0 V	0.60	1.04	1.50	0.60	1.70	V
		V_{CC} = 4.5 V	1.00	1.55	2.00	1.00	2.20	V
		V_{CC} = 5.5 V	1.20	1.86	2.30	1.20	2.50	V
V_H [2]	hysteresis voltage	see Figure 9, Figure 10 and Figure 11						
		V_{CC} = 1.8 V	0.15	0.49	1.00	0.15	1.20	V
		V_{CC} = 2.3 V	0.25	0.60	1.10	0.25	1.30	V
		V_{CC} = 3.0 V	0.40	0.73	1.20	0.40	1.40	V
		V_{CC} = 4.5 V	0.60	0.92	1.50	0.60	1.70	V
		V_{CC} = 5.5 V	0.70	1.02	1.70	0.70	1.90	V

[1] All typical values are measured at T_{amb} = 25 °C

[2] $V_H = V_{T+} - V_{T-}$

12. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

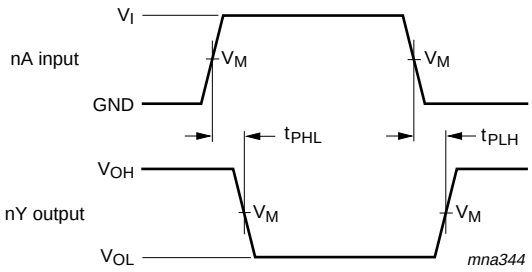
Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 7	[2]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.2	11.0	1.0	12.0	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	3.0	6.5	0.5	7.2	ns
		V_{CC} = 2.7 V		0.5	3.8	7.0	0.5	7.7	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	3.2	6.0	0.5	6.7	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.4	4.3	0.5	4.7	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V	[3]	-	18.1	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

13. Waveforms

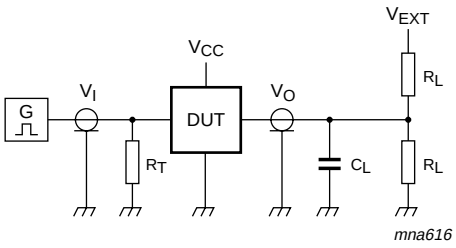


Measurement points are given in Table 10. V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The data input (nA) to output (nY) propagation delays

Table 10. Measurement points

V_{CC}	Input V_M	Output V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in Table 11. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuitry for switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

14. Waveforms transfer characteristics

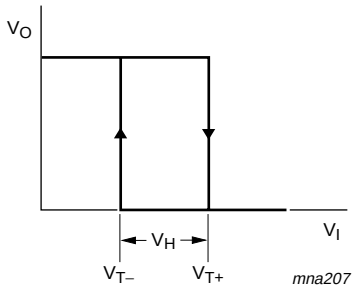
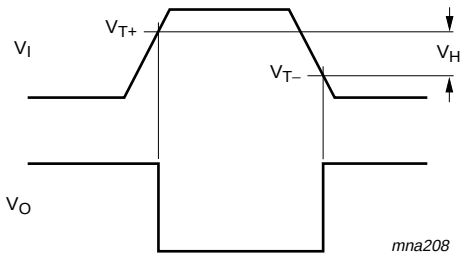
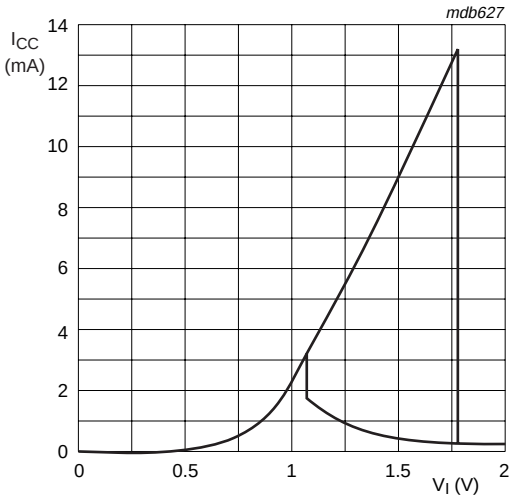


Fig 9. Transfer characteristic



V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig 10. Definition of V_{T+}, V_{T-} and V_H



V_{CC} = 3.0 V

Fig 11. Typical transfer characteristics

15. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (µW);

f_i = input frequency (MHz);

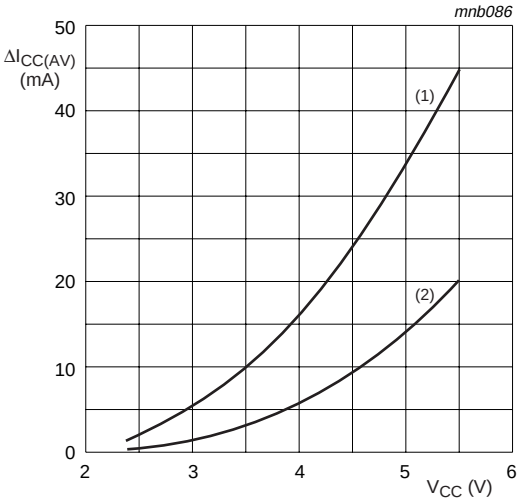
t_r = input rise time (ns); 10 % to 90 %;

t_f = input fall time (ns); 90 % to 10 %;

$\Delta I_{CC(AV)}$ = average additional supply current (µA).

$\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Figure 12.

An example of a relaxation circuit using the 74LVC3G14 is shown in Figure 13.

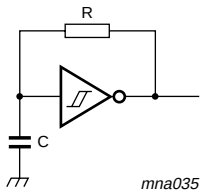


Linear change of V_I between 0.8 V to 2.0 V. All values given are typical unless otherwise specified.

(1) Positive-going edge.

(2) Negative-going edge.

Fig 12. $\Delta I_{CC(AV)}$ as a function of V_{CC}

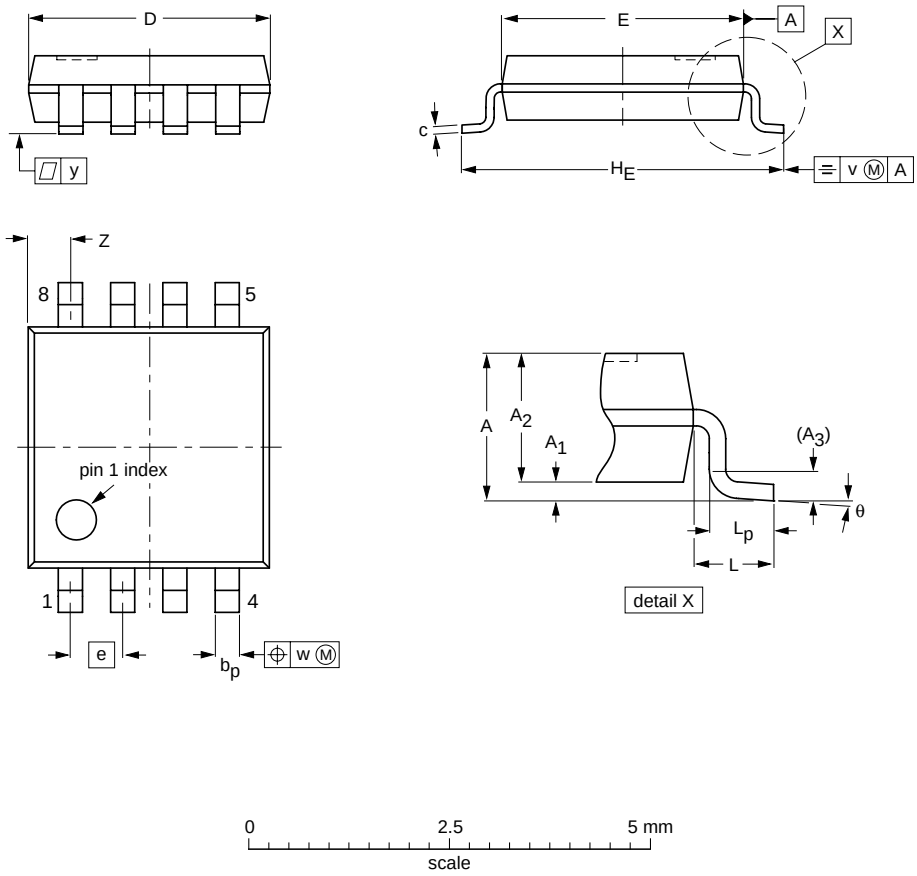


$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Fig 13. Relaxation oscillator

16. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

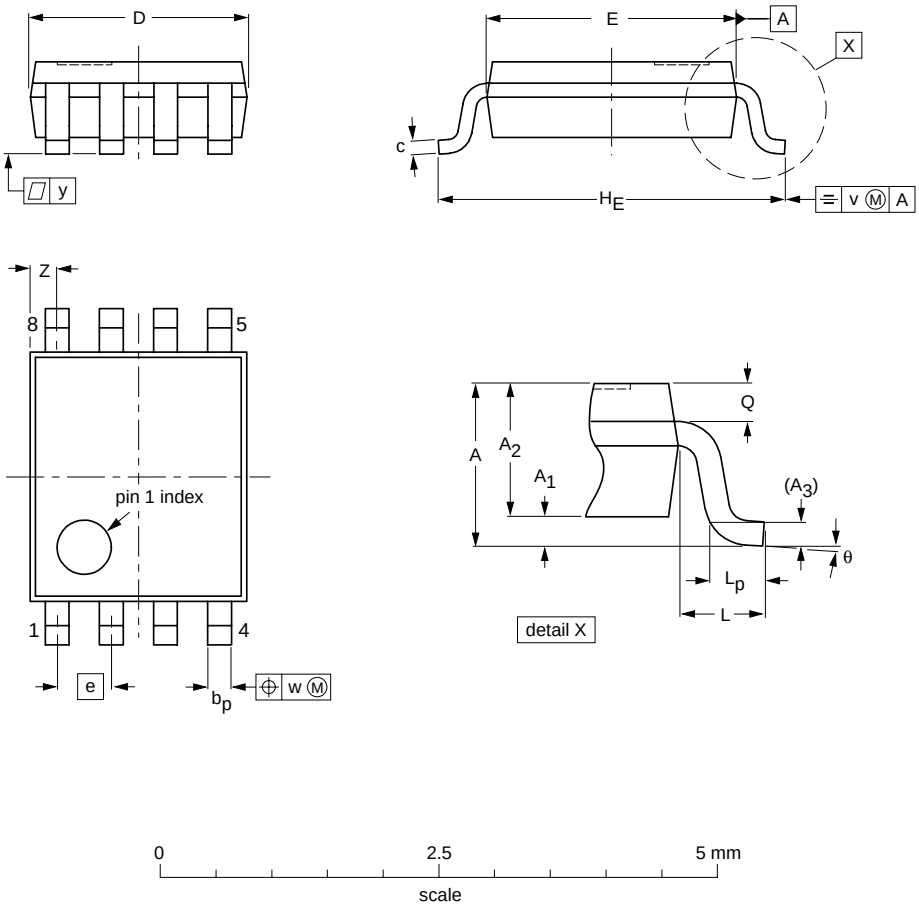
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 14. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

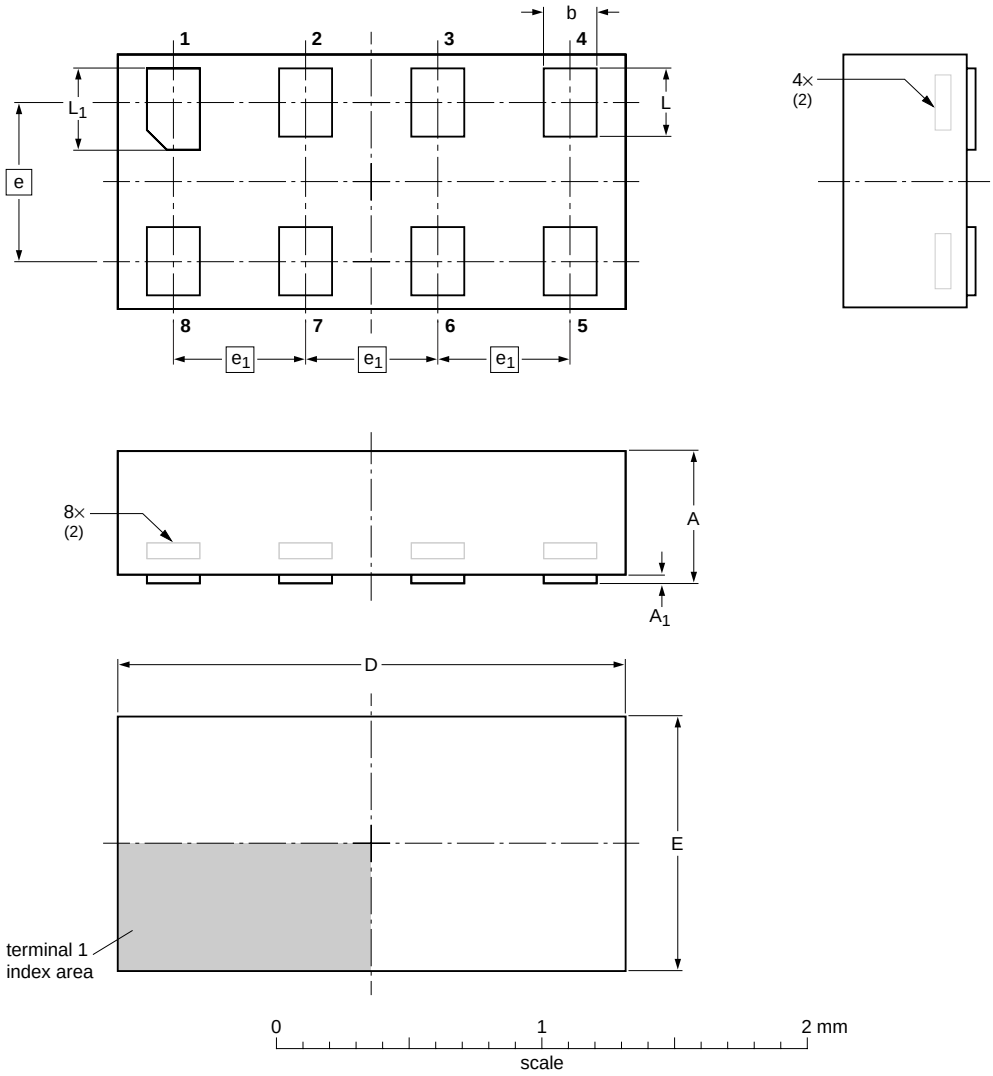
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 15. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

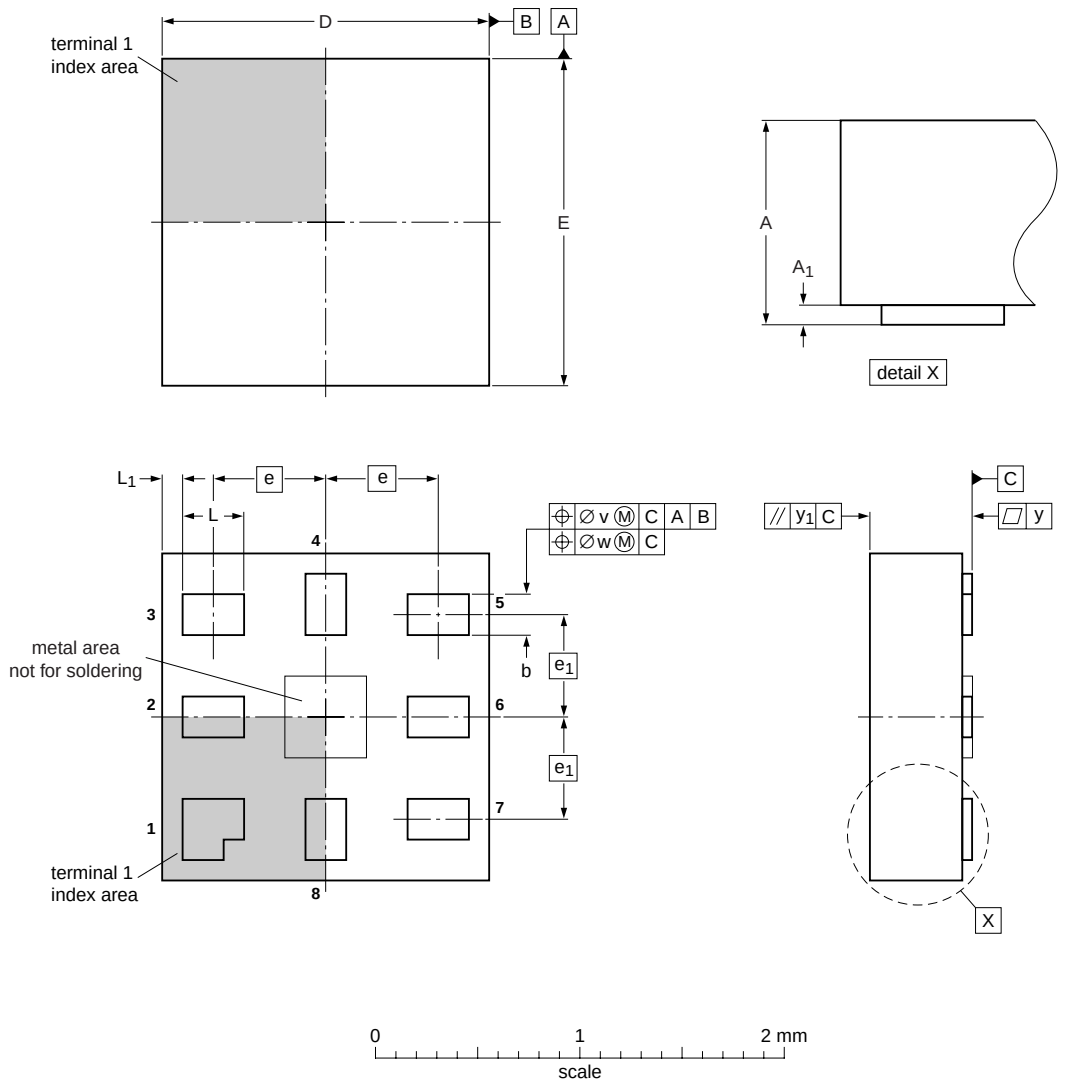
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 16. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm **SOT902-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT902-1	- - -	MO-255	- - -			~~05-11-25~~ 07-11-14

Fig 17. Package outline SOT902-1 (XQFN8U)

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3G14_6	20080207	Product data sheet	-	74LVC3G14_5
Modifications:	• Figure 17: package outline drawing updated to latest version • Figure 1 and Figure 2: pin numbers removed from logic symbols			
74LVC3G14_5	20071005	Product data sheet	-	74LVC3G14_4
74LVC3G14_4	20070314	Product data sheet	-	74LVC3G14_3
74LVC3G14_3	20050131	Product data sheet	-	74LVC3G14_2
74LVC3G14_2	20041027	Product data sheet	-	74LVC3G14_1
74LVC3G14_1	20040510	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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